Claims:

1. A programmable integrated circuit, comprising:

a. a bus;

b. a processor, connected to said bus, for performing digital filtering on digital signals;

c. a data interface, connected to said bus, for receiving external digital signals having respectively different characteristics for filtering by said processor; and

d. a serial data output register, for receiving filtered digital signals from said processor and providing them to an output port.

2. The integrated circuit of claim 1, further comprising at least one test modulator, connected to said bus, for generating a test signal having a controlled delay.

3. The integrated circuit of claim 2, in which said at least one test modulator is programmable to selectively generate a test signal using different algorithms.

4. The integrated circuit of claim 1, further comprising a serial control interface.

5. The integrated circuit of claim 1, further comprising a serial peripheral interface.

6. The integrated circuit of claim 1, further comprising a general purpose Input/Output interface.

7. The integrated circuit of claim 1, in which said processor is configured to provide programmable decimation and filtering.

8. The integrated circuit of claim 1, in which said data interface provides an output selectively to one of two different sinc filters.

9. The integrated circuit of claim 1, in which separate power supplies are provided respectively to said data interface, said processor and to said serial data output register.

10. The integrated circuit of claim 1, formed on an integrated circuit.

11. The integrated circuit of claim 10, in which said integrated circuit includes a token input pin and a token output pin.

12. A plurality of programmable digital filters of claim 11, serially connected from token output pin of one integrated circuit to token input pin of the next integrated circuit in which the token input pin of a first programmable digital filter is connected to a microcontroller and the token output pin of a last programmable digital filter is connected to said microcontroller.

13. The programmable digital filter of claim 1, in which the cells of the serial data output register not needed for delay are operated in a reduced power mode.

14. The programmable digital filter of claim 13, in which power is removed from said cells not needed for delay during said reduced power mode.

15. A method of designing an integrated circuit, comprising the steps of:

a. providing for a bus;

b. providing for a processor, connected to said bus, for performing digital filtering on digital signals;

c. providing for a data interface, connected to said bus, for receiving external digital signals having respectively different characteristics for filtering by said processor; and

d. providing for a serial data output register, for receiving filtered digital signals from said processor and providing them to an output port.

16. A method of fabricating an integrated circuit, comprising the steps of:

a. providing a bus;

b. providing a processor, connected to said bus, for performing digital filtering on digital signals;

c. providing a data interface, connected to said bus, for receiving external digital signals having respectively different characteristics for filtering by said processor; and

d. providing a serial data output register, for receiving filtered digital signals from said processor and providing them to an output port.